

Development of Orderly Micro Asperity on Polishing Pad Surface for Chemical Mechanical Polishing (CMP) Process using Anisotropic Etching

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Abstract

CMP is one of the most essential processes in ULSI manufacture. However, the polishing characteristics during CMP remain unidentified because pad surface roughness such as asperity or texture is complicated and random. Thus, this study specifies the orderly micro asperity arrayed on surface of a polishing pad instead of complicated random asperity on conventional pad, in order to discuss and to improve the polishing performance. Particularly, design of surface geometry on polishing pad is proposed and then its orderly micro patterned pad has been firstly developed by applying lithographic technology, which is commonly used in MEMS manufacturing process. The orderly micro pyramidal asperity's design has 12 μm pitch with base width of $7 \times 7 \mu\text{m}^2$ and 4.95 μm height. Next our developed pad surface was 3D-microscopically observed. The dimension errors of the micro pyramid were less than 0.5 μm . Furthermore, the duplicating process of the micro patterned pad also has been developed for mass production trial. Finally, the developed pads were employed in CMP experiments in order to compare the material removal characteristic of the micro pyramidal asperity pad with a conventional pad. As the experimental results, the MRR (material removal rate) of the developed pad trended similar to that of a conventional pad, and the unobservable MRR of non-asperity pad, implying efficiency of the orderly asperity.

Keywords: *Polishing pad, Anisotropic, Etching, CMP, Asperity*

1 Introduction

Chemical Mechanical Polishing (CMP) is one of most important processes used in the semiconductor manufacturing industry to achieve the flatness of the substrate, which is necessary for constructing multilevel interconnection in Ultra Large Scale Integration (ULSI). Figure 1 illustrates the schematic of CMP process with microscopic region between a polishing pad and a wafer during polishing. A wafer is pressed and rotated onto a polishing pad settled on a rotating platen; simultaneously polishing slurry (chemical solution with nano-sized fine particles) is supplied to the polishing pad surface. The CMP mechanism is generally explained that mechanical motion in process removes the very thin material layer, which is weakened by chemical reaction of slurry component [1-5]. However, the material removal mechanism in CMP process is still not identified absolutely [5].

One of many actions in CMP, the mainly mechanical action concerns the relative movement between polishing pad surface and wafer surface, particularly in the microscopic region. In this study, one of the most essential mechanical parameters, the functionality of asperity on the polishing pad surface, has been discussing. As it is well known that the asperity on the pad is complicated and random, the concrete discussion for functionality of asperity becomes difficult. In this paper, non-randomly orderly asperity polishing pads have to be developed in order to enable discussion the pad's polishing functionality. Next, the CMP experiments employing the developed pad were carried out to verify the necessity of asperity on a polishing pad and compare material removal rate (MRR) to the conventional generally-use pad. In addition, the duplicating

process of the micro patterned pad is also introduced for mass production trial.

2 Orderly micro asperity on polishing pad

2.1 Structure of conventional polishing pad

The structure of the conventional generally-used polishing pad in CMP process is illustrated in figure 2. Polishing pad has 20-50 micrometers size of pore based on porous polyurethane material. The pad also contains randomly distributed asperity as shown in the enlarged wafer adjoining area in figure 2 [1-4]. It is well known that changes in pad asperity, so-called roughness, affect the removal of material from the wafer surface or the material removal rate (MRR). Particularly, the MRR would be high when the average asperity height arithmetical mean roughness (Ra) is 4 μm approximately [6]. However, these polishing pad random structures are difficult to control stably in practical.

2.2 Design of the orderly asperity

Since the asperity on the pad is random, discussion of functionality of the pad surface in CMP process is difficult in general. In this work, one of the most essential parameters, the asperity on polishing pad surface, is discussed. Non-randomly designed polishing pad with orderly pyramidal asperity on the pad surface have been developing in order to enable discussion of the pad's polishing functionality.

The designed polishing pad composed of polyurethane material is shown in figure 3. By the specification limit of lithography devices to be employed, the polishing pad would have been fabricated on 4 inches (101.6 mm) silicon wafer in diameter. The wafer would be provided as a mold of the designed pad to be fabricated. The micro pyramidal asperity shape was also preferred because of constraint geometry by anisotropic silicon etching.

In order to expect the high MRR as mentioned in previous subsection, the micro pyramid asperity height was set at 4.95 μm , slightly larger than 4 μm , by the reasons of the errors occurring in casting and molding process, and the constraint of anisotropic etching geometry. Subsequently, the orderly micro pyramid base width was set at 7 μm and the pitch was set at 12 μm as shown in figures 3.

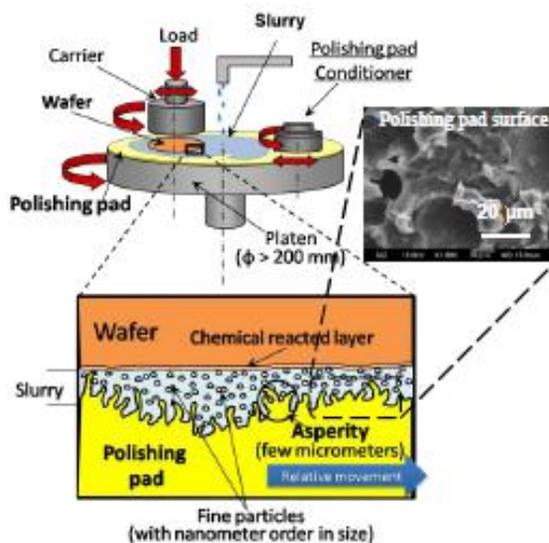


Figure 1: Schematic of CMP process

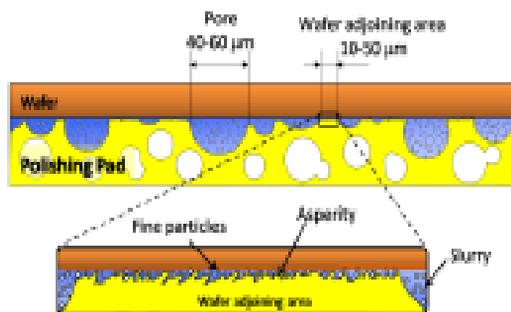


Figure 2: Illustrating between wafer and pad surface during CMP

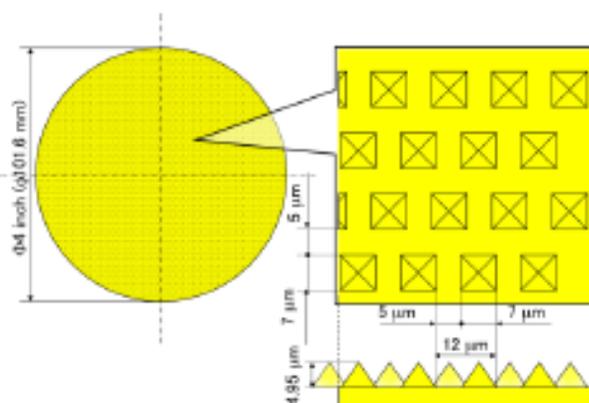


Figure 3: Design of the micro pyramidal asperity

3 Fabrication of orderly asperity polishing pad

3.1 Anisotropic etching of crystalline silicon

It is well known that etching rate of the (111) face of silicon in KOH aqueous solution is much lower than that of other faces, particularly when comparison to the (100) face [7]. The (100) face of silicon wafer is lithographed in this work; therefore the constraint geometry of anisotropic etching (in procedure number 8 of next subsection) is shown in figure 4. Considering the design of micro pyramid base b is 7 μm , and the angle θ between (100) and (111) face is 54.74 degree constrainedly, the etched pit depth h becomes 4.95 μm .

3.2 Fabrication procedure employing lithography

Figure 5 shows a fabrication procedure of our designed polishing pad with orderly asperity. The process applies lithography technology that commonly used in MEMS manufacturing as followings;

- (1) Fabricate the photomask printed the periodical pattern of the above mentioned micro array's width and pitch.
- (2) Clean the crystalline silicon wafer to be used as a substrate for providing the designed pad's mould.
- (3) Grow up SiO_2 layer on the substrate surface.
- (4) Coat photoresist on the grown up SiO_2 layer.
- (5) Expose g-line ($\lambda = 436 \text{ nm}$) from ultraviolet

lamp pass through the pre-made photomask toward the photoresist on the substrate aligned by an aligner, and then remove unhardened photoresist.

- (6) Etch off the un-photoresist-covered region in SiO_2 layer.
 - (7) Remove remaining photoresist.
 - (8) Perform anisotropic etching of the crystalline silicon substrate in un- SiO_2 -covered surface to form micro etched pit by KOH solution.
 - (9) Remove remaining SiO_2 .
- Note: Si wafer mould with reverse periodical pattern is ready.
- (10) Cast polyurethane into the ready mould.
 - (11) Peel the hardened polyurethane out of the mould.

Furthermore, the silicone rubber moulding die was also provided by using the fabricated original orderly asperity polishing pad as illustrating in figure 6.

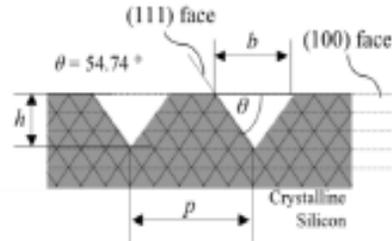


Figure 4: Constraint micro etched pits on crystalline silicon substrate

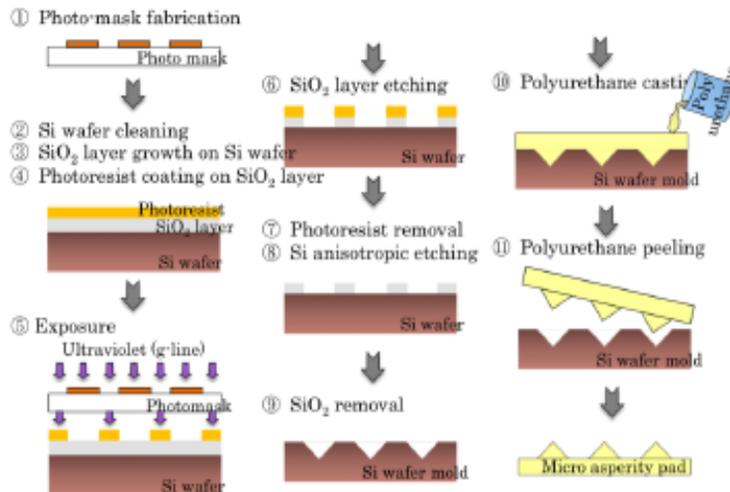


Figure 5: Fabrication procedure of orderly asperity polishing pad

3.3 Fabricated polishing pad

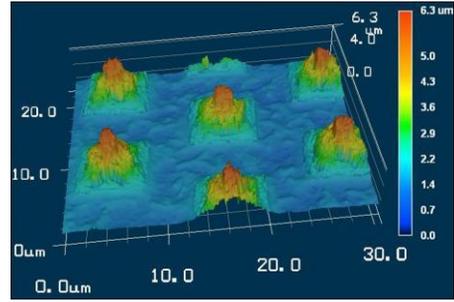
Figure 7(a) and (b) displays the observation results of the developed orderly asperity pad surface provided by silicon wafer mould, as shown in figure 5. Figure 7(a) shows the observed images from Confocal Laser Scanning Microscope (CLSM; Keyence: VK-9700) and figure 7(b) shows the images from electron-beam three-dimensional roughness analyzer (3D-SEM; ELIONIX: ERA-8800). Figure 7(c) displays the trial twice duplicated polishing pads provided by the silicone rubber mould, as shown in figure 6. The results from both different measuring instruments and from twice duplicating process notified that the orderly pyramidal asperity was mostly fabricated similarly to the designed dimensions.

The details of the observed results (6 times measurement) are shown in table 1. The averaged pyramidal based width was $7.37 \mu\text{m}$, 5% wider than the designed size, with dimension distribution of $\pm 4\%$ approximately. The averaged height was $4.54 \mu\text{m}$, 8% shorter than the designed size, with dimension distribution of $\pm 10\%$ approximately. The averaged micro pyramid pitch was $11.82 \mu\text{m}$, 1.5% closer than the designed size, with dimension distribution of $\pm 8\%$ approximately. The developed duplicated polishing pad would be employed in CMP experiments for verifying the polishing performance, comparison to the IC1000 pad, the most generally-used polishing pad.

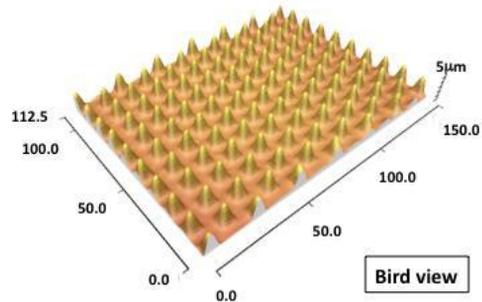
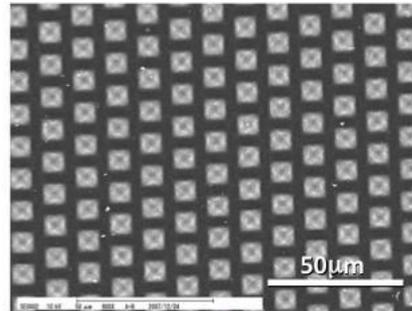
4 CMP experiments

4.1 Experimental

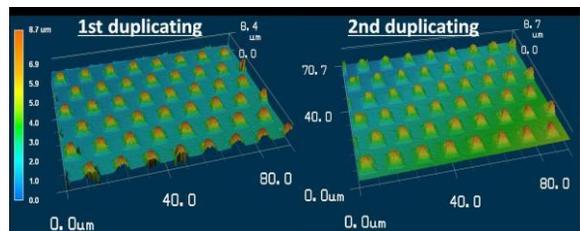
In order to evaluate the polishing performance of the developed orderly asperity polishing pad, the CMP experiments of SiO_2 coated wafers were carried out employing 3 types of polyurethane polishing pads as



(a) CLSM image of original pad



(b) 3D-SEM image of original pad



(c) CLSM images of the twice duplicated pads

Figure 7: 3D microscopic observation of the fabricated polishing pad surface

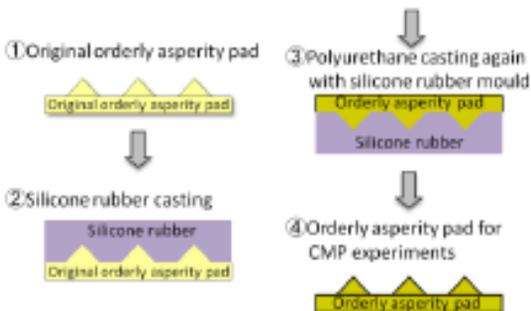


Figure 6: Duplicating process of the developed polishing pad

Table 1: Dimension of orderly asperity

Geometry	Design length [μm]	Observed length [μm]
Base width	7	7.37 (7.04 to 7.59)
Height	4.95	4.54 (4.09 to 5.07)
Pitch	12	11.82 (10.85 to 12.55)

followings; (i) conventional generally-used porous pad (IC 1000), (ii) the developed non-porous pad with orderly asperity and (iii) non-porous pad without asperity. The CMP experimental conditions are shown in Table 2 and the experimental set up is shown in figure 8. The polishing pads to be experimented with diameter of 101.6 mm were set at centre of the platen of a polishing machine (Maruto instruments: Doctor Lap ML-180S).

The material removals were evaluated by decrease of the silica film thickness after experiments with ellipsometer (Rudolph Instruments: Auto EL IV NIR-3). The material removals were averaged from 9 points measurement on the wafer, one point at the centre of a wafer and other 8 points (at the 4 middle points between wafer centre and each wafer edge sides and at the 4 edge points).

4.2 Results and discussions

The material removal rate of the developed polishing pad was evaluated in SiO₂-coated wafer CMP experiments. Table 3 shows the material removal in the experiments with 3 types of polyurethane polishing pads (n/a means Not Available value due to unstable polished surfaces). It is implied that the indispensability of the asperity on pad surface was verified; because changes of SiO₂ layer thickness was unable to be observed when the pad surface had no asperity. Figure 9 also shows the material removal and their rates respectively, particularly in comparison between conventional IC1000 pad and the developed pad.

As the CMP experimental results corresponding to polishing time as shown in figure 9, the material removal tendency of the developed pad was similar to the conventional pad. The developed pad played the MRR to be slightly larger than of the conventional pad at the beginning of CMP. However, the MRR of the conventional pad was more stable than of the developed pad. These results mentioned the functionality of the periodically orderly pyramidal asperity on polishing pad surface.

Nevertheless, the MRRs in both cases considerably decreased after starting CMP for 4-5 minutes due to degradation of both pads, particularly in the developed pad as shown in figure 10. This pad degradation, namely the decrease of asperity height, induced decrease of the MRR. In other words, it is implied that the height of asperity on the polishing pad surface influences the polishing characteristics.

Table 2: CMP experimental conditions

Work piece	□ 20 mm of SiO ₂ -coated wafers
Polishing pad (Polyurethane)	(i) IC1000
	(ii) With orderly asperity
	(iii) Without asperity
Slurry	12.5wt% of SiO ₂ in pH 11 KOH solution
Pad and Wafer revolution	60 min ⁻¹
Polishing pressure	34.5 kPa (5 psi)
Polishing time	0, 1, 3, 5, 7 min
SiO ₂ layer thickness	Ellipsometer(Rudolph Instruments:Auto EL IV NIR-3)

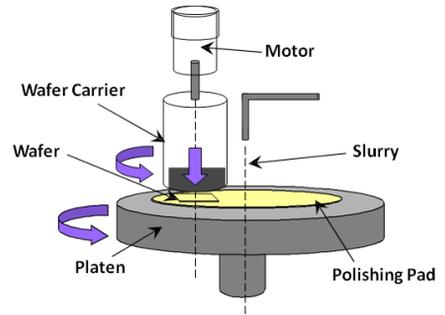


Figure 8: CMP experimental setup

Table 3: Material removals [in nanometre] from decreasing of SiO₂ layer thickness on polished wafers

Polishing time	1 min	3 min	5 min	7 min
IC1000	15.5	n/a	76.7	83.8
Orderly asperity pad	14.7	69.7	n/a	94.1
Pad without asperity	n/a	≡0	n/a	≡0

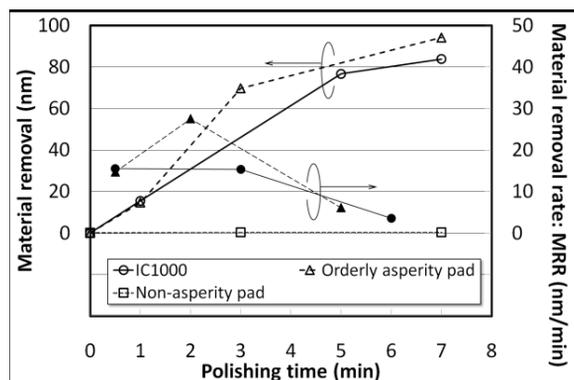


Figure 9: Material removal change with CMP time

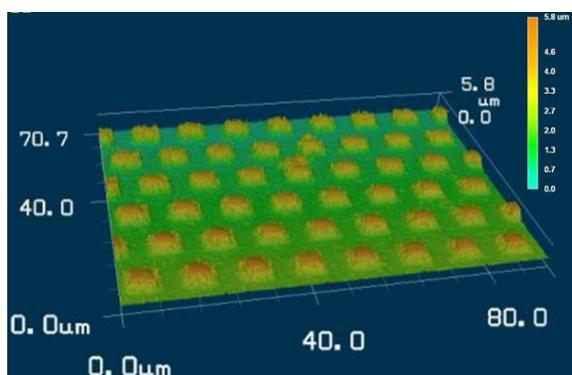


Figure 10: Degradation of the developed orderly asperity pad after 3 minutes polishing

5 Conclusions

This study aims to clarify the necessity and functionality of conventionally randomly distributed asperity on the polishing pad surface by comparing with orderly distributed asperity. The lithography technique was applied to providing the micro pattern mould for fabrication of polishing pads with orderly asperity. The duplicating process also has been developed for mass-production trial. By employing the developed pads in CMP experiments, it is verified firstly that the designed and fabricated pad with array asperity, based on the pad roughness data, played comparable MRR with the conventional pad. Next the asperity on pad surface is indispensable for CMP process because unobservable MRR of non-asperity pad. Finally, degradation of asperity height decreases the MRR.

References

- [1] Lee S., Kim K. and Dornfeld D., 2005. *Development of a CMP pad with controlled micro features for improved performance*, Proc of IEEE international Symposium on Semiconductor Manufacturing, ISSM 2005: 173-176.
- [2] Park B., Lee H., Park K, Kim K. And Jeong H., 2008. *Pad roughness variation and its effect on material removal profile in ceria-based CMP slurry*, J. Mater. Process. Technol., 203 (1-3): 287-292.
- [3] McGrath J. and Davis C., 2004. *Polishing pad surface characterization in chemical mechanical planarisation*, J. Mater. Process. Technol., 153-154: 666-673.
- [4] Lu H., Fookes B. Machinski S. and Richardson K., 2002. *Quantitative analysis of physical and chemical changes in CMP polyurethane pad surfaces*, Materials Characterization, 49(1): 35-44.
- [5] Kimura K., Hashiyama Y., Khajornrungruang P., Hiyama H. and Mochizuki Y., 2007. *Study on material removal phenomena in CMP process*, Proc of International Conference on Planarization/CMP technology, ICPT 2007: 201-205.
- [6] Planarization and CMP Technical Committee, 2006. *A library of CMP planarization Technology & Application*, Global Net Corp: 483. [in Japanese]
- [7] Philipsen H., Smeenk N. Ligthart H. and Kelly J., 2006. *Exploiting Anisotropy for In Situ Measurement of Silicon Etch Rates in KOH Solution*, Electrochemical and Solid-state Letters, 9(7): C118-C121.